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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/651,599	DAVIS, RAYMOND A..	
	Examiner	Art Unit	
	Hung H. Lam	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09/27/07.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-36 and 41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-36 and 41 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 29 August 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date: _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 09/27/2007, have been entered and made of record. Claim 37 is canceled. Claims 1-36 and 38-41 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-35 and 38-41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

"portions of the first and second image data are selectively blocked at each respective image module to synchronize the first and second image data received by

the circuitry on the substrate" in independent claims 1, 17 and 38 are not described or shown in originally filed specification.

"wherein portions of the first and second images are selectively blocked at each respective image module to synchronize the first and second images displayed on the screen" in independent claim 31 is not described or shown in originally filed specification.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 31 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beckett (US-5,852,502).

With regarding **claim 31**, Beckett discloses an electronic apparatus, comprising:
a substrate (it is inherent a substrate is inherent included in the electronic camera system of Fig. 4);

a first image module (24) adapted to capture a first image mounted said substrate (Fig. 4)

a second image module (22) adapted to capture a second image mounted on a said substrate (see Fig. 4); and

a screen (94) coupled to the substrate and adapted to display the first and second images captured by said first and second image modules (Col. 8, Ln. 10-56).

wherein portions of the first and second images are selectively blocked at each respective image module to synchronize the first and second images displayed on the screen (abstract; Col. 7, Ln. 30-68).

wherein portions of the first and second image data are selectively blocked at each respective image module to synchronize the first and second image data received by the circuitry on the substrate (Col. 7, Ln. 30- Col. 8, Ln. 56).

With regarding **claim 38**, Monroe discloses a method of operating an electronic apparatus the electronic apparatus including first and second image modules having first and second outputs (Fig. 4; 36 and 34), respectively, said method comprising

capturing first and second scenes, as first and second data streams, using the first image module and the second image module (abstract;), respectively;

transmitting the first image data stream to circuitry on a substrate via at least one common data line (see the output of Mux 45) and the first output of the first image module (Col. 7, Ln. 30-68);

transmitting the second image data stream to the circuitry on the substrate via the at least one common data line and the second output of the second image module (Col. 7, Ln. 30-68); and

synchronizing the first and second image data streams received by the circuitry on the substrate by selectively blocking reception of portions of the first and second

image data streams transmitted by the first and second outputs (abstract; Col. 7, Ln. 30-68), respectively via at least one common data line to the circuitry on the substrate, to generate a composite image data stream (abstract; Col. 7, Ln. 30-Col. 8, Ln. 56).

5. Claims 36 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Monroe (US-7,057,647).

With regarding **claim 36**, Monroe discloses a method of operating an electronic apparatus having first and second image modules, said method comprising:

capturing a scene the first image module (Figs. 6 and 9; imager 100) while the second image module (imager 104) is not operating (see mux 112);
previewing the scene on a display (Figs. 2-5; view finder 20);
turning on the second image module after the capturing of the scene by the first image module (Col. 6, Ln. 38-66; Col. 7, Ln. 60-Col. 8, Ln. 15); and

capturing, after the turning on of the second image module previewing, the scene at a higher resolution than the previewed scene using the second image module based on the previewed scene (Col. 6, Ln. 38-66; Col. 7, Ln. 60-Col. 8, Ln. 15: Monroe teaches different imager 100-124 having different zoom values).

With regarding **claim 38**, Monroe discloses a method of operating an electronic apparatus the electronic apparatus including first and second image modules having

first and second outputs (Figs. 6 and 9; see camera Address and Data), respectively, said method comprising

capturing first and second scenes, as first and second data streams, using the first image module and the second image module (Figs. 6 and 9; see camera 100-104 or imager140 146), respectively;

transmitting the first image data stream to circuitry on a substrate via at least one common data line and the first output of the first image module (Col. 6, Ln. 38-66; Col. 7, Ln. 60-Col. 8, Ln. 15);

transmitting the second image data stream to the circuitry on the substrate via the at least one common data line and the second output of the second image module (Col. 6, Ln. 38-66; Col. 7, Ln. 60-Col. 8, Ln. 15); and

synchronizing the first and second image data streams received by the circuitry on the substrate by selectively blocking reception of portions of the first and second image data streams transmitted by the first and second outputs (Col. 6, Ln. 38-66; Col. 7, Ln. 60-Col. 8, Ln. 15; it is inherent that when a camera is selected, other camera data transmission are blocked), respectively via at least one common data line to the circuitry on the substrate, to generate a composite image data stream (Col. 6, Ln. 38-66; Col. 7, Ln. 60: composite image data stream inherently form on the camera data bus when 106 or 150 when the plurality of imagers or cameras are transmitted data to the bus one by one).

With regarding **claim 39**, Monroe discloses the method wherein the composite image data stream is generated on a shared tri-state bus (see Fig. 6).

With regarding **claim 40**, Monroe discloses a the method recited in claim 38, wherein the synchronizing of the first and second image data streams is based on a portion of the first scene defining a window-of-disinterest (Col. 6, Ln. 38-66; Col. 7, Ln. 60-Col. 8, Ln. 15).

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
7. Claims 1-8, 10-11, 13-14 and 17-22, 26-27, 30 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake (US-2001/0,050,721) in view of Johnson (US-2006/0,197,847) and further in view of Larson (US-2004/0,252,642).

With regarding **claim 1**, Miyake discloses a dual camera module comprising:
a substrate having circuitry thereon for receiving image data (Figs. 22A-22B;
image sensors 2; wires 11);
a first image module for capturing first image data, and including a first output for transmitting the first image data to the circuitry on the substrate module (Figs. 22A-22B; image sensors 2; wire 11; [0008; 0149]);

a second image module for capturing second image data, and including a second output for transmitting the second image data to the circuitry on the substrate (Figs. 22A-22B; image sensors 2; [0008; 0149]); and
a flex interconnect (0161-0162; 0236).

However, Miyake fails to explicitly disclose a flex interconnect having a common data line that is shared by the first and second image modules, the common data line being configured to electrically connect the first and second outputs to the circuitry on the substrate.

In the same field of endeavor, Johnson teaches an image processor system wherein I2C bus is used for allowing multiple cameras to be connected together (0128). Johnson further teaches that a respective data processing subsystem includes registers, which are configured according to the present invention to share a common address space (0014). In light of the teaching from Johnson, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake by including an I2C bus in a flexible printed circuit board in order to allow multiple cameras to be connected together and thereby simplify camera circuitry.

However, Miyake and Johnson fails to explicitly disclose wherein portions of the first and second image data are selectively blocked at each respective image module to synchronize the first and second image data received by the circuitry on the substrate.

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In the same field of endeavor, Larson teaches an apparatus for transmitting data from a first and second I2C source port buffer (abstract). Larson further teaches a step for transmitting the data from the first I2C source port buffer to the I2C destination port while restricting transmission form the second I2C source port buffer to the I2C destination port (Fig. 9; step 903; [0103-0106]). In light of the teaching from Larson, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake and Johnson by selectively restricting transmission form a respective I2C source port buffer to the I2C destination port while transmitting the data from an alternative I2C source port buffer to an I2C destination port. The modifications thus prevent data collision and improve the I2C bus communication.

With regarding **claim 2**, Miyake in view of Johnson and further in view of Larson discloses a dual camera module further comprising: control lines and further data lines (Miyake: Figs. 22A-22B; wires 11; 0236) and at least one component on the flex interconnect that are shared by the first and second image modules (Johnson: 0014; 0128).

With regarding **claim 3**, Miyake in view of Johnson and further in view of Larson discloses a dual camera module each of the image modules comprises a lens and an image sensor (Miyake: lens 3a and image sensor 2; 0015-0017; 0109-0120).

With regarding **claim 4**, Miyake in view of Johnson and further in view of Larson discloses the dual camera module wherein each of the image modules comprises a lens (Miyake: 3a) and a combination imaging sensor (Miyake: 2) and image processor (Miyake: 0149: teaches a designated peripheral element such that ASIC or DSP is used).

With regarding **claim 5**, Miyake in view of Johnson and further in view of Larson discloses the dual camera module wherein the first image module faces a first direction and the second image module faces a second direction (Miyake: see image sensors 2 in Figs. 22A-22B).

With regarding **claim 6**, Miyake in view of Johnson and further in view of Larson discloses the dual camera module wherein said each of the image modules are uniquely addressable (Johnson: 0128: it is inherent that each camera is programmed with a unique I2C address in order to distinguish each one of the multiple cameras).

With regarding **claim 7**, Miyake in view of Johnson and further in view of Larson fails to disclose the dual camera module wherein said both of the image modules respond to a common or global address (Johnson: 0014; 0128).

With regarding **claim 8**, Miyake in view of Johnson and further in view of Larson fails to explicitly disclose the dual camera module wherein said flex interconnect includes an Inter-IC (I2C) bus (Johnson: 0014; 0128).

With regarding **claim 10**, Miyake in view of Johnson and further in view of Larson discloses the dual camera module wherein each of the image modules is programmed to respond to a unique Inter-IC (I2C) address (Johnson: 0128: it is inherent that each camera is programmed with a unique I2C address in order to distinguish each one of the multiple cameras).

With regarding **claim 11**, the claim contains the same limitations as claimed in claim 7. Therefore, claim 11 is analyzed and rejected as claim 7.

With regarding **claim 13**, Miyake in view of Johnson and further in view of Larson discloses the dual camera wherein a first image module captures images at a first resolution and the second image module captures images at a second resolution (Miyake: Figs. 22A-22B; 0161-0162: it is inherent that both image sensors 2 capture images at first and second resolution).

With regarding **claim 14**, Miyake in view of Johnson and further in view of Larson discloses the dual camera module wherein a first image module captures images having a first orientation and a second image module captures images having a second orientation (Miyake: see Figs. 22A-22B; 0161-0162).

With regarding **claim 17**, Miyake discloses an electronic apparatus comprising:
a substrate having circuitry thereon for receiving image data (Figs. 22A-22B;
substrate 1; [0161]); and
a dual camera module connected to said substrate, said dual camera module
adapted to capture images, the dual camera module including
a first image module (2) adapted to capture a first image in a first direction (Figs.
22A-22B; [0161-0162]) and including a first output for transmitting the first captured
image to the circuitry on the substrate (wires 11).
a second image module (2) adapted to capture second image in a second
direction (Figs. 22A-22B; [0161-0162]) and including a second output for transmitting
the second captured image to the circuitry on the substrate (wires 11), and
data lines (0161-0162; 0236).

However, Miyake fails to explicitly disclose a common set of data lines that are
shared by the first and second image modules, the common set of data lines being
configured to electrically connect the first and second outputs to the circuitry on the
substrate.

In the same field of endeavor, Johnson teaches an image processor system
wherein I2C bus is used for allowing multiple cameras to be connected together
(0128). Johnson further teaches that a respective data processing subsystem includes
registers, which are configured according to the present invention to share a common
address space (0014). In light of the teaching from Johnson, it would have been

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obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake by including an I2C bus in a flexible printed circuit board in order to allow multiple cameras to be connected together and thereby simplify camera circuitry.

However, Miyake and Johnson fails to explicitly disclose wherein portions of the first and second captured images are selectively blocked at each respective image module to synchronize the first and second captured images received by the circuitry on the substrate.

In the same field of endeavor, Larson teaches an apparatus for transmitting data from a first and second I2C source port buffer (abstract). Larson further teaches a step for transmitting the data from the first I2C source port buffer to the I2C destination port while restricting transmission form the second I2C source port buffer to the I2C destination port (Fig. 9; step 903; [0103-0106]). In light of the teaching from Larson, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake and Johnson by selectively restricting transmission form a respective I2C source port buffer to the I2C destination port while transmitting the data from an alternative I2C source port buffer to an I2C destination port. The modifications thus prevent data collision and improve the I2C bus communication.

With regarding **claim 18**, the claim contains the same limitations as claimed in claim 3. Therefore, claim 18 is analyzed and rejected as claim 3.

With regarding **claim 19**, the claim contains the same limitations as claimed in claim 4. Therefore, claim 19 is analyzed and rejected as claim 4.

With regarding **claim 20**, Miyake in view of Johnson and further in view of Larson discloses the electronic apparatus wherein each of the image modules further comprises an imaging filter (Miyake : [0236]).

With regarding **claim 21**, Miyake in view of Johnson and further in view of Larson discloses the electronic apparatus wherein the first direction and the second direction are opposite directions relative to each other (Miyake : see Figs. 22A-22B; 0161-0162).

With regarding **claim 22**, the claim contains the same limitations as claimed in claim 8. Therefore, claim 22 is analyzed and rejected as claim 8.

With regarding **claim 26**, the claim contains the same limitations as claimed in claim 7. Therefore, claim 26 is analyzed and rejected as claim 7.

With regarding **claim 27**, Miyake discloses the electronic apparatus further comprising a screen for displaying the captured images (0211; 0214-0216; 0244).

With regarding **claim 30**, the claim contains the same limitations as claimed in claim 13. Therefore, claim 30 is analyzed and rejected as claim 13.

With regarding **claim 41**, Miyake in view of Johnson and further in view of Larson discloses the dual camera module recited in claim 1, wherein: the first and second image modules have a shared, common housing and include first and second imaging arrays, respectively (Miyake: 0161-0162; 0236; Johnson: [0014;0128]); and the flex interconnect attaches the shared, common housing to the substrate and electrically connects the first and second imaging arrays to the circuitry of the substrate (Miyake: Figs. 22A-22B; Johnson: [0014;0128]).

8. Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake (US-2001/0,050,721) and further in view of Larson (US-2004/0,252,642).

With regarding **claim 31**, Miyake discloses an electronic apparatus, comprising:
a substrate (Figs. 22A-22B; substrate 1);
a first image module adapted to capture a first image mounted said substrate (Figs. 22A-22B; image sensors 2; [0008; 0149]);
a second image module adapted to capture a second image mounted on a said substrate (Figs. 22A-22B; image sensors 2; [0008; 0149]); and
a screen coupled to the substrate and adapted to display the first and second images captured by said first and second image modules (0211; 0214-0216; 0244).

wherein portions of the first and second images are selectively blocked at each respective image module to synchronize the first and second images displayed on the screen.

However, Miyake fails to explicitly disclose wherein portions of the first and second image data are selectively blocked at each respective image module to synchronize the first and second image data received by the circuitry on the substrate.

In the same field of endeavor, Larson teaches an apparatus for transmitting data from a first and second I2C source port buffer (abstract). Larson further teaches a step for transmitting the data from the first I2C source port buffer to the I2C destination port while restricting transmission form the second I2C source port buffer to the I2C destination port (Fig. 9; step 903; [0103-0106]). In light of the teaching from Larson, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake by selectively restricting transmission form a respective I2C source port buffer to the I2C destination port while transmitting the data from an alternative I2C source port buffer to an I2C destination port. The modifications thus prevent data collision and improve the I2C bus communication.

With regarding **claim 32**, Miyake in view of Larson discloses the electronic apparatus further comprising a screen for displaying the first and second captured images (Miyake: 0211; 0214-0216; 0244).

With regarding **claim 33**, Miyake in view of Larson discloses a dual camera module each of the image modules comprises a lens and an image sensor (Miyake: lens 3a and image sensor 2; 0015-0017; 0109-0120).

With regarding **claim 34**, Miyake in view of Larson discloses the dual camera module wherein each of the image modules comprises a lens (Miyake: 3a) and a combination imaging sensor (Miyake: 2) and image processor (Miyake: 0149: teaches a designated peripheral element such that ASIC or DSP is used).

With regarding **claim 35**, Miyake in view Larson discloses the dual camera module wherein the first image module faces a first direction and the second image module faces a second direction (Miyake: see image sensors 2 in Figs. 22A-22B).

9. Claims 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Johnson, in view of Larson and further in view of Kayada (US-2004/0,119,718).

With regarding **claim 12**, Miyake in view of Johnson and further in view of Larson fails to explicitly disclose the dual camera module wherein the first and second image modules are each configured to tri-state an output signals.

In the same field of endeavor, Kayada teaches a camera system wherein the camera input switching section outputs a signal to turn on/off the output of a tri-state

buffer to thereby switch between imaged data from the two camera modules (0051). In light of the teaching from Kayada, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake, Johnson and Larson by including the switching section and output tri-state buffer in order to switch between imaged data from two camera modules (Kayada: 0051).

10. Claims 9 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Johnson, in view of Larson and further in view of Stam (US-2004/0,230,358).

With regarding **claim 9**, Miyake in view of Johnson and further in view of Larson fails to disclose the dual camera module wherein said flex interconnect includes a Serial Peripheral Interface (SPI).

In the same field of endeavor, Stam teaches image sensor side LVDS transceivers which are integrated into an imager (Fig. 9c; 901c) along with other components (0260). This integration thus reduces the part count, component cost and imager board area associated with image sensor side LVDS transceivers (0260). Stam further teaches that the communication protocols such that a serial bus, LVDS serial bus, SPI bus or IIC bus may be used to transmit data from the imager to the processor or from the processor to the imager (0260). In light of the teaching from Stam, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake, Johnson and Larson by integrating a serial bus, LVDS

serial bus, SPI bus or IIC into an imager along with other components. The modifications thus reduce the part count, components cost and imager board area and provide communication between imager and processor (Stam: 0260).

With regarding **claim 23**, the claim contains the same limitations as claimed in claim 9. Therefore, claim 23 is analyzed and rejected as claim 9.

With regarding **claim 24**, the claim contains the same limitations as claimed in claim 9. Therefore, claim 24 is analyzed and rejected as claim 9.

11. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Johnson, in view of Larson, in view of Stam and further in view of Tanha (US-2002/0,108,011).

With regarding **claim 25**, Miyake in view of Johnson, in view of Larson and further in view of Stam fails to disclose the electronic apparatus wherein each of the image modules is programmed to respond to a unique slave select signal on the SPI bus.

In the same field of endeavor, Tanha teaches a dual interface serial bus wherein the same slaves address is used by a device 400 regardless of the protocol selected (I2C or SPI). Tanha further teaches that this saves on having separate slave address registers for each protocol as is done in the prior art (0018). In light of the teaching

from Tanha, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake, Johnson, Larson and Stam by using the same slaves address regardless of the protocol selected from I2C or SPI. The modifications thus reduce separate slave address-registers (Tanha:0018).

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Johnson, in view of Larson and further in view of Monroe (US-7,057,647).

With regarding **claim 15**, Miyake in view of Johnson, in view of Larson fails to explicitly disclose the dual camera module wherein the first image module captures images of a first color range and the second image module captures images of a second color range.

In the same field of endeavor, Monroe teaches a dual mode camera having a color image sensor for daylight operation and a monochrome image sensor for nighttime operation (Fig. 1; Col. 5, Ln. 49-59). In light of the teaching from Monroe, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake in view of Johnson, in view of Larson by having monochrome and color image sensor in order to perform daylight and night time operation. The modifications thus allow the camera to capture better images in the day and night time.

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13. Claims 16 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Johnson, in view of Larson and further in view of Kuroda (US-2003/0,036,365).

With regarding **claim 16**, Miyake in view of Johnson, in view of Larson fails to explicitly disclose the dual camera module wherein the first image module has a first focal length and a second image module has a second focal length.

In the same field of endeavor, Kuroda teaches a dual mode camera having a close-range photography camera module in one side and long-range photography camera module in the opposite side (abstract; 0034-0035; close and long range photography camera modules inherently comprise a first and second focal length). In light of the teaching from Kuroda, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake, Johnson and Larson by having a close-range photography camera module in one side and long-range photography camera module in the opposite side. The modifications thus reduce the used of shaft mechanism and wiring complication and thus ensuring the reliability of the camera (Kuroda: 0007-0009).

With regarding **claim 29**, the claim contains the same limitations as claimed in claim 16. Therefore, claim 29 is analyzed and rejected as claim 16.

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14. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Johnson, in view of Larson and further in view of Wells (US-2004/0,179,600).

With regarding **claim 28**, Miyake in view of Johnson, in view of Larson fails to explicitly disclose the electronic apparatus further comprising a screen coupled to the circuitry on the for simultaneously displaying the first captured image from the first image module synchronized with the second captured image from the second image module.

In the same field of endeavor, Wells teaches an imaging system (Fig. 7; 100') wherein one of the output signals ENCa to ENCk may be generated to contain conventional picture-in-picture (PIP) type resolution video streams for normal "digest" viewing of multiple cameras (0028). Wells further teaches the output signal ENC may be multiplex to one of the output video signals for viewing on a single monitor screen (0028). In light of the teaching from Wells, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Miyake, Johnson and Larson by multiplexing the video output of the multiple cameras for viewing PIP on a single monitor screen. The modifications thus provide a more versatile camera.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, LIN YE can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



TUAN HO
PRIMARY EXAMINER

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HL
12/07/07